UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,509	01/12/2001	Gilbert Wolrich	10559/317001/P9678	2157

20985 7590 10/04/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,509	WOLRICH ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2004 and 12 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 15-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 15-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 and 15-26 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 6/09/04, Extension of Time as received on 8/12/04, and Amendment A as received on 8/12/04.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5 and 15-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Parady, U.S. Patent No. 5,933,627.

7. Regarding claims 1 and 15, taking claim 1 as exemplary, Parady has taught an execution unit for execution of multiple context threads comprises:

a. An arithmetic logic unit to process data for executing threads (see Col.2 lines 18-29 and Col.3 lines 19-25),

b. Control logic to control the operation of the arithmetic logic unit (see Col.3 lines 10-18),

c. A general purpose register set (48 of Fig.1/Fig.3) to store and obtain operands for the arithmetic logic unit, the register set constructed with a two-ported random access memory architecture, with the register set divided into a plurality of banks (see Col.3 lines 43-49), each bank having two ports and capable of performing a read and a write to two different words with the two ports in the same processor cycle (see Fig.3 and Col.3 lines 43-49). Here, because the register file contains ten ports (see 48 of Fig.1) and four banks (see Col.3 lines 43-49), there are inherently at least two ports per bank, therefore allowing each bank to write or read at least one word per bank per cycle.

8. Claim 15 is nearly identical to claim 1, differing in its parent claim, but encompassing the same scope. Therefore, claim 15 is rejected for the same reasons as claim 1.

9. Regarding claims 2 and 16, taking claim 2 as exemplary, Parady has taught the execution unit of claim 1, wherein the register set is logically partitioned into a plurality of relatively addressable windows (see Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is

divided into four register files for four threads (see Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (see Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field.

10. Claim 16 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope. Therefore, claim 16 is rejected for the same reasons as claim 2.

11. Regarding claims 3 and 17, taking claim 3 as exemplary, Parady has taught the execution unit of claim 2, wherein the number of windows of the register set is according to the number of threads that can execute in the processor (see Col.3 lines 43-49).

12. Claim 17 is nearly identical to claim 3, differing in its parent claim, but encompassing the same scope. Therefore, claim 17 is rejected for the same reasons as claim 3.

13. Regarding claims 4, 18 and 21, taking claim 4 as exemplary, Parady has taught the execution unit of claim 1, where the relative addressing allows the currently executing thread to access to any of the registers relative to the starting point of a window of registers (see Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is divided into four register files for four threads (see Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (see Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field, allowing a thread to access registers associated with its 2-bti thread field.

14. Claims 18 and 21 are nearly identical to claim 4, differing in their parent claims, but encompassing the same scope. Therefore, claim 18 and 21 are rejected for the same reasons as claim 4.

15. Regarding claims 5 and 22, taking claim 5 as exemplary, Parady has taught the execution unit of claim 1, wherein the register set is absolutely addressable where any one of the addressable registers may be accessed by the currently executing thread by providing the exact address of the register (see Col.3 lines 43-49 and Col.4 lines 1-8, 18-22). As shown above in paragraphs 23 and 27, the register set is relatively addressable using a 2-bit thread field that specifies which thread, and consequently which register window, an instruction's operands come from. However, the 2-bit thread field can also be used to inter-relate two threads (see Col.4 lines 18-22), thus allowing one thread to access to any other register in any other thread, providing absolute addressability.

16. Claim 22 is nearly identical to claim 5, differing in its parent claim, but encompassing the same scope. Therefore, claim 22 is rejected for the same reasons as claim 5.

17. Regarding claim 19, Parady has taught a processor unit comprising:

a. An execution unit for execution of multiple context threads comprising:

I. An arithmetic logic unit to process data for executing threads (see Col.2 lines 18-29 and Col.3 lines 19-25),

II. Control logic to control the operation of the arithmetic logic unit (see Col.3 lines 10-18),

III. A general purpose register set (48 of Fig.1/Fig.3) to store and obtain operands for the arithmetic logic unit (see Fig.3), the register set constructed with a two-ported random access memory architecture, the register set being arranged into a plurality of banks (see Col.3 lines 43-49), each bank having two ports (see Fig.3 and Col.3 lines 43-49). Here,

because the register file contains ten ports (see 48 of Fig. 1) and four banks (see Col.3 lines 43-49), there are inherently at least two ports per bank.

18. Regarding claim 20, Parady has taught the processor of claim 19, wherein the register set is logically partitioned into a plurality of relatively addressable windows where the number of windows of the register set is according to the number of threads that can execute in the processor (see Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is divided into four register files for four threads (see Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (see Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 6-7 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 as applied to claims 1-5 above, and further in view of Waldspurger et al., "*Register Relocation: Flexible Contexts for Multithreading*".

21. Regarding claims 6 and 23, taking claim 6 as exemplary, Parady has taught the execution unit of claim 1, wherein the control logic further comprises:

a. Context switching logic (112 of Fig.3) fed by signals from a plurality of shared resources (see Col.3 lines 57-65).

22. Parady has not explicitly taught wherein the signals cause the context event logic to indicate that threads are either available or unavailable for execution.

23. However, Waldspurger has taught a context switch scheduler that comprises a circularly-linked "ready queue" which determines which contexts are ready for execution when a context switch is required in order to provide fast context switching (see paragraph 1 of Sec. 2.2). One of ordinary skill in the art would have recognized that it is a primary goal of microprocessor designers to reduce delays in their datapath, such as those introduced when a context switch is required, thereby increasing the speed and throughput of their processors. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to provide threads that are available for execution in the manner of Waldspurger so that context switches can be performed fast, thus increasing the processor speed.

24. Regarding claims 7 and 23, taking claim 7 as exemplary, Parady in view of Waldspurger has taught the execution unit of claim 6, wherein the control logic addresses a set of memory locations for storing a list of available threads that correspond to threads that are ready to be executed and a set of memory locations for storing a list of unavailable threads that are not ready to be executed (see above paragraph 37 and Waldspurger paragraph 1 of Sec. 2.2). Here, the "set of memory locations" is a circularly-linked queue, such that the next threads that are ready to be executed are at the "head" of the list, while those that are not ready, or were recently switched from, reside at the "tail" of the list (see Waldspurger Sec. 2.2).

25. Claim 23 is nearly identical to claims 6 and 7, differing in its parent claim, but encompassing the same scope as claims 6 and 7. Therefore, claim 23 is rejected for the same reasons as claims 6 and 7.

26. Regarding claim 24, Parady in view of Waldspurger has taught the processor of claim 23, wherein execution of a context swap instruction causes a currently running thread to be swapped out to the unavailable thread memory set and a thread from the available thread memory set to begin execution within a single execution cycle (see Parady Fig.3, Col.2 lines 18-25, Col.3 lines 57-65 and Waldspurger paragraphs 2-5 of Sec. 2.2.). Here, a load or store operation signals a context switch (see Parady Fig.3 and Col.3 lines 57-65), and the context switch steps store the current context at the "tail" of the circularly-linked list and update the current context to be the thread that was next in line to be executed (see Waldspurger paragraphs 2-5 of Sec. 2.2).

27. Regarding claim 25, Parady in view of Waldspurger has taught the processor of claim 23, wherein execution of the context swap instruction specifies one of the signal inputs and upon receipt of the specified signal input causes the swapped out thread to be stored in the available thread memory set (see Parady Fig.3, Col.2 lines 18-25, Col.3 lines 57-65 and Waldspurger paragraphs 2-5 of Sec. 2.2.). Here, a load or store operation signals a context switch (see Parady 114 of Fig.3 and Col.3 lines 57-65), and the context switch steps store the current context at the "tail" of the circularly-linked list and update the current context to be the thread that was next in line to be executed (see Waldspurger paragraphs 2-5 of Sec. 2.2).

28. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady in view of Waldspurger as applied to claim 23 above, and further in view of Trauben et al., U.S. Patent No. 5,509,130.

29. Regarding claim 26, Parady in view of Waldspurger has taught the processor of claim 23, but have not explicitly taught wherein execution of the context swap instruction specifies a defer_one operation which causes execution of one more instruction and then causes the current context to be swapped out.

30. However, Trauben has taught a branch delay instruction which causes the execution of one instruction before changing context in order to hide the latency of computing and fetching the branch target (see Col.14 lines 41-60). One of ordinary skill in the art would have recognized that it is desirable to reduce the amount of delay in a microprocessor and thus allow faster execution times. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Waldspurger to include a branch delay instruction which allows an instruction to execute while computing and fetching a branch target so that the latency of the operation can be avoided.

Response to Arguments

31. Applicant's arguments filed 8/12/04 have been fully considered but they are not persuasive.

32. On p.8 of the present Amendment, the Applicant argues with respect to claims 1-5 and 15-22, essentially:

> *"Parady discloses a typical register file architecture, e.g., integer registers 48 in Fig.1. The integer registers 48 include 8 windows for 4 threads and include 10 ports. However, in the embodiment described in the Specification, the register file set having the dual-ported RAM architecture supports four threads (p.3 line 8), 8 windows (Fig.6), and only*

requires 4 ports (two for each of banks A and B). Furthermore, a search of the text of Parady indicates that the terms "random access memory" and "RAM" are not even mentioned."

33. The Applicant is correct in noting that the integer register file of Parady can be divided in up to 8 windows, and does in fact contain 10 ports (see 48 of Fig.1). However, the embodiment that the Examiner used in the previous rejection (see paragraph 21 of rejection mailed on 3/09/04), and repeated again above (see paragraph 7 above), the register file is divided into separate banks for each thread (see Col.3 lines 47-49). Because the register file does have 10 ports, there are inherently at least two ports per bank. Thus, the integer register file of Parady has taught, "the register set divided into a plurality of banks, each bank having two ports and capable of performing a read and a write to two different words with the two ports in the same processor cycle".

34. Further, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the register file supporting "4 threads, 8 windows, and only requires 4 ports") are not recited in the rejected claim(s). The claim language only states "a register set constructed with a two-ported random access memory architecture, with the register set divided into a plurality of banks, each bank having tow ports and capable of performing a read and a write to two different words with the two ports", and makes no statements as to the amounts of threads, windows, or total ports required to implement it. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

35. Finally, the Applicant's argument regarding Parady not disclosing the terms "random access memory" or "RAM" is confusing, as the Applicant is not claiming a RAM at all, but simply a register set having a dual-ported RAM "architecture". This is further confusing as a register set is something wholly different from a RAM, and no difference in the terminology is claimed. Regardless of the terminology used, a RAM has an architecture that allows data of a specific length to be read from or written to it based on an address. This is the same operation as a register file, with the main difference being that the register file is generally smaller in total size and physically and logically closer to the execution units of a processor. However, no such claims are made of the "register file set having a dual-ported Ram architecture", and thus Parady has taught such a feature.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. After October 12th, 2004, the examiner can be reached at (571) 272-4171. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm, with the exception of first Friday of every bi-week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached at (703) 305-9712, or at (571) 272-4162 on or after October 12th, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
10/1/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100